

REMARKS

The Office Action of December 30, 2005 has been received and its contents carefully considered.

The present Amendment adds a new dependent claim 19 to further protect the invention. It is supported (for example) by element 16, shown in Figure 1 of the present application's drawings.

The Office Action rejects independent claim 1 (the sole independent claim in this application) for obviousness based on patent 5,598,430 to Hachisuka et al (which will hereafter be called simply "Hachisuka") in view of patent 5,151,922 to Weiss. This rejection is respectfully traversed, for the reasons discussed below.

Claim 1 recites a demodulator for demodulating received radio signals into digital signals, and "a mode selector for selecting either of a reproduction mode of reproducing the digital signals and an evaluation mode of evaluating the digital signals." The Office Action characterizes Hachisuka's switch 112 as the "mode selector" of claim 1. This conclusion is respectfully traversed.

Hachisuka's switch 112 selects either a digital signal from a digital signal detecting circuit 108 or an analog signal from an FM signal detecting circuit 107 in response to the output of a logic discriminating circuit 111. The output of Hachisuka's logic discriminating circuit 111 is based on information from a noise detecting circuit 109 and an RSSI detecting circuit 110. Hachisuka's noise detecting circuit 109 detects whether the noise component in the output from the FM detecting circuit 107 is less than a specified value, and his RSSI detecting circuit 110 uses the output from an intermediate frequency amplifier 106 to determine whether the received signal strength is less than a

specified value (see column 4 of the reference, lines 4-37). In other words, Hachisuka's arrangement judges whether a received signal is analog or digital based on the received signal strength and noise in the signal from FM signal detecting circuit 107, and then Hachisuka's switch 112 connects the proper detecting circuit (that is, either the digital signal detecting circuit 108 or the FM signal detecting circuit 107) to an amplifier 113. The reference teaches that this arrangement avoids a time delay that was required in the past (see, for example, column 1, lines 62-64 and column 2, lines 6-9).

To the extent that Hachisuka's switch 112 can be characterized as a mode selector, the modes that it selects are clearly either a digital reproduction mode or an FM analog reproduction mode. An ordinarily skilled person would have had no reason to think that Hachisuka's switch 12 selects either a reproduction mode of reproducing digital signals or "an evaluation mode of evaluating the digital signals" in accordance with claim 1.

Claim 1 also recites "an error generator for inverting a level of the digital signals for the evaluation mode at a predetermined timing to generate error data." The Office Action acknowledges that Hachisuka does not teach inverting the level of a digital signal, but points to the Weiss reference. The Office Action takes the position that it would have been obvious to implement the teachings of Hachisuka into Weiss in order to disable the speaker while a data signal is present. (It is noted that this rationale leaves it unclear which reference is considered to be the primary reference and which is considered to be a secondary reference.) At any rate, the rationale advanced in the Office Action is not supported by the references, since an ordinarily skilled person would understand that Hachisuka's digital signal detecting circuit 108 outputs an audio signal that can be

switched (by Hachisuka's switch 112) to an audio amplifier 113 in order to drive a speaker 115. That is, Hachisuka's arrangement is able to select a digital signal for driving his speaker 115; Hichisuka does not disable his speaker 115 when a digital signal is present.

Weiss teaches that a demodulated signal is coupled to a filter 12 and a limiter 14 to provide a signal that is fed to a data detector 15. A digital signal, which indicates the presence or absence of a data signal, is emitted from the data detector 15 to an inverter 64, whose output is supplied to one input of an AND gate 61. The output of AND gate 61 is used to mute a speaker 6 when a data signal is present (see column 3, lines 16-28).

In summary, Hachisuka's switch 112 selects either a digital signal or an FM analog signal, in contrast to the "mode selector" recited in claim 1. In addition, the inverter 64 in the Weiss reference is used for disabling an amplifier so as to mute a speaker while a data signal is present. This is quite different from the "error generator" recited in claim 1. An ordinarily skilled person would have had no reason to combine the teachings of these references but, even assuming for sake of argument that the teachings were combined, they would not have led an ordinarily skilled person to the invention defined by claim 1.

The remaining claims depend directly or indirectly from claim 1 and recite additional limitations to further define the invention, so they are patentable along with claim 1 and need not be further discussed. Nevertheless, claim 2 and new dependent claim 19 will now be briefly addressed.

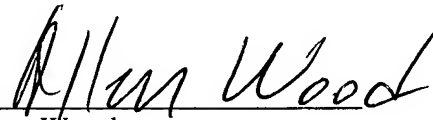
The Office Action rejects claim 2 for obviousness on the basis of Hachisuka and Weiss, and further in view of Shinozaki et al (hereafter simply "Shinozaki"). The Office

Action draws attention to Figure 6 of the reference, and to the selectors 164 and 168 in Figure 6.

Claim 2 provides that the "mode selector" of claim 1 comprises first and second selectors. However, an ordinarily skilled person would have had no reason to think that Shinozaki's selectors 164 and 168 select "either of a reproduction mode of reproducing the digital signals or an evaluation mode of evaluating the digital signals" in accordance with claims 1 and 2 together. Nor do Shinozaki's selectors 164 and 168 represent "a pair of single pole, double throw switches that are connected to one another, both switches being responsive to a common selection signal" in accordance with new claim 19.

For the foregoing reasons, it is respectfully submitted that this application is in condition for allowance. Reconsideration of the application is therefore respectfully requested.

Respectfully submitted,



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